Power GaAs MESFET with a High Drain-Source Breakdown Voltage

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Abstract—**A power GaAs MESFET with a high drain-source breakdown voltage in excess of 17 V has been developed. A selective GaAs epitaxial process is introduced to form "inlaid" n^+ source and drain regions that can provide a high drain-source breakdown voltage and a low ohmic-contact resistance. Typical characteristics of the MESFET composed of two-cell units are as follows:**

$P_{1\,dB}$ = 2.2 W G_L = 4.2 dB η_{add} = 21.6% at 8 GHz

$P_{1\,dB}$ = 2.7 W G_L = 6.0 dB η_{add} = 30.7% at 6 GHz

$P_{1\,dB}$ = 4.0 W G_L = 7.0 dB η_{add} = 43.5% at 4 GHz

where $P_{1\,dB}$, G_L, and η_{add} indicate the output power at 1-dB gain compression, linear gain, and power added efficiency, respectively. The intercept point for third-order intermodulation products is 41.5 dBm at 6.2 GHz.

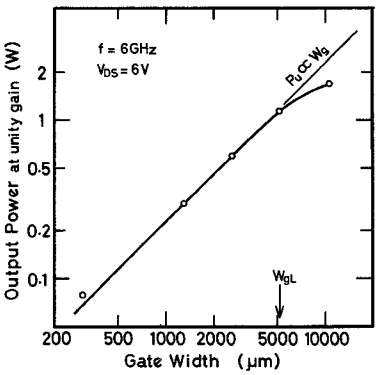

Fig. 1. Relation between output power P_u at unity gain and total gate width W_g at 6 GHz.

I. INTRODUCTION

THE GaAs MESFET has useful gain with low noise in the frequency range where Si bipolar transistors remain ineffective.

Following successful results in low-noise and wide-band applications [1] it has been demonstrated that the GaAs FET has excellent potential as a microwave power device [2]–[9]. At the beginning of 1973, the GaAs MESFET showed its possibility [2], [3], and at the end of 1974 it became the first three-terminal solid-state device that broke through a barrier of 1-W output power in *X* band [6]. Recently, it was reported that the GaAs MESFET showed not only good efficiency but also its inherent linearity [9]. The good efficiency and linearity are desirable for many applications in the field of communication. The output power level of state-of-the-art GaAs MESFET's is, however, lower than that of *L*-band Si bipolar transistors.

This paper presents a power GaAs MESFET with a high drain-source breakdown voltage. Its design considerations, geometry, fabrication process, and performance are described. The device can produce 4 W in *C* band and 2.2 W in *X* band.

II. DESIGN CONSIDERATIONS

A. Practical Limit of the Total Gate Width

One of the methods to realize a high-power FET may be to design a FET pattern with a wide gate that can control a large drain current. However, there is a maximum gate width beyond which the voltage along the gate becomes nonuniform. The maximum width can be estimated from the criterion that the transmission line formed by the source and gate electrodes should be less than a 1/10 wavelength. For example, the maximum gate width for a 1-μm-long gate is calculated to be about 50 μm at 10 GHz [6]. Since the uniform gate voltage is desirable for efficient operation, a number of 50-μm-wide gates are connected in parallel to obtain a total gate width necessary for controlling a large drain current.

An experimental result shown in Fig. 1 indicates that output power at unity gain P_u is proportional to total gate width W_g up to the point indicated by W_{gL}. A MESFET with a gate wider than W_{gL} delivers less output power than expected from a linear dependence on total gate width. This may be understandable since a wider gate causes nonuniform distribution of RF power among component MESFET's. W_{gL} may be determined by dimensional variations among the component FET's and the nonuniformity of the GaAs epitaxial layer.

B. Drain-Source Breakdown Voltage

Another method to increase the output power is to design a FET "structure" with a high drain-source breakdown voltage (V_{dsB}). A high V_{dsB} allows a high drain-source bias voltage (V_{ds}). Another experimental result is shown in Fig. 2. The P_u of a 5200-μm-wide gate MESFET increases with V_{ds}. In this experiment V_{ds} in excess of 9 V could not be applied because of a breakdown phenomenon between the drain and source. If a higher bias voltage could be applied, it would be possible to get a higher output power proportional to the bias.

Fig. 3(a) shows the drain-source breakdown of Sample A. Sample A has Au–Ge alloyed planar electrode as the source and drain, and an n-type channel without a gate. The source periphery and separation between the source

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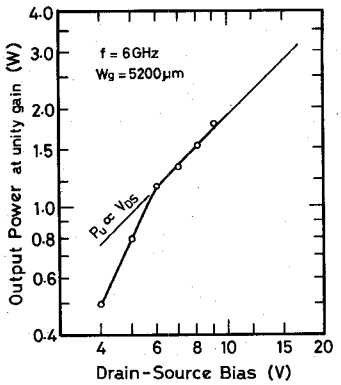

Fig. 2. Relation between output power P_u at unity gain and drain-source bias voltage V_{ds} at 6 GHz.

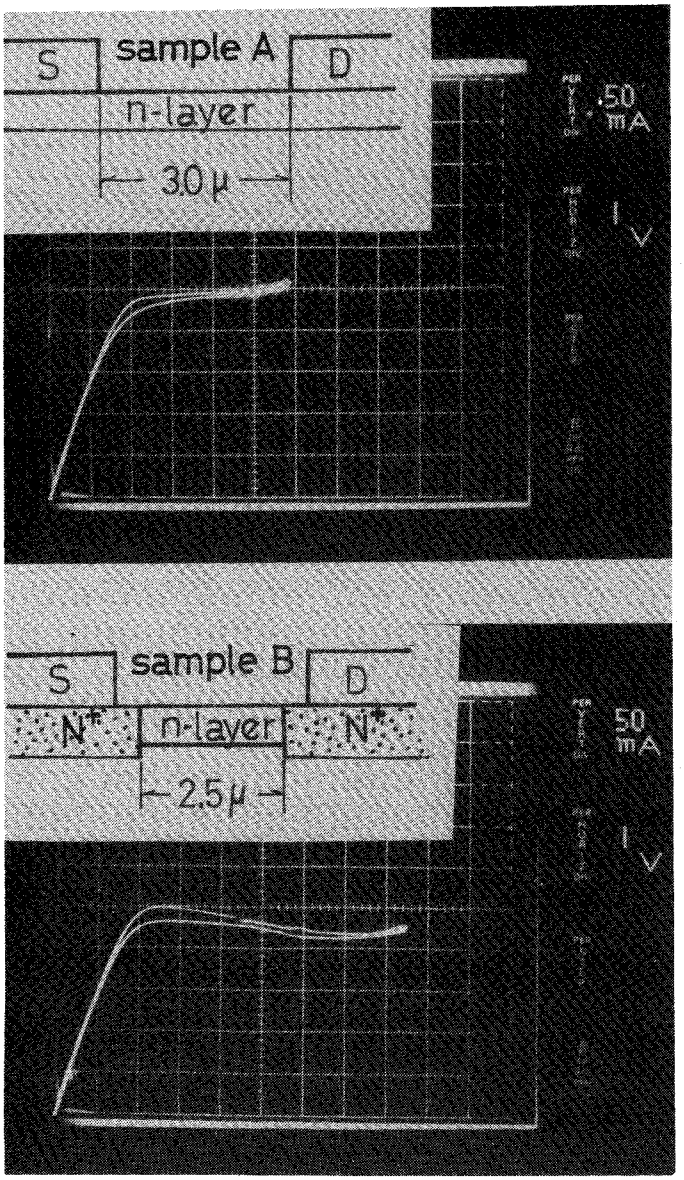

Fig. 3. (A) Drain-source breakdown of Sample A without inlaid n^+ regions. (B) Drain-source breakdown of Sample B with inlaid n^+ regions.

and drain are 300 and 3 μm, respectively. The doping density and thickness of the n-type layer are 1×10^{17} cm^{-3} and 0.2 μm, respectively. The drain-source breakdown voltage V_{dsB} of Sample A is much lower than anticipated from the theoretical breakdown field (40 V/μm) of GaAs [10] times the distance between the source and drain. This can be explained as follows. The drain-source breakdown takes place near the edges of the planar contacts where the electric field becomes considerably higher than the average field strength.

In order to reduce the field near the contacts, "inlaid" n^+ regions are introduced under the source and drain electrodes in Sample B, of which the drain-source breakdown is shown in Fig. 3(b). A fabrication process of the inlaid n^+ regions will be described in detail in the following section. The source periphery, doping density, and thickness of Sample B are the same as those of Sample A, except for the separation between the source and drain ($\sim$ 2.5 μm), which is slightly shorter. It is clearly seen that the average breakdown field of Sample B (4 V/μm) is considerably higher than that of Sample A (1.7 V/μm). These data show that V_{dsB} is closely related to the source and drain configurations.

These experiments give useful information to design a power MESFET as follows.

1) There is a practical limit W_{gL} in total gate width. With our present technology W_{gL} is about 5000 μm.

2) If V_{ds} higher than 15 V is applied to a MESFET with $W_g \simeq 5000$ μm, it will be possible to obtain a P_u as high as 3 W at 6 GHz as estimated from Fig. 2.

3) It is possible to improve V_{dsB} by the introduction of inlaid n^+ regions under the source and drain electrodes.

III. Geometry and Fabrication Process

A. Pattern Design

Considering the preceding results and our present technical level, single-cell and two-cell MESFET's were designed for 6-GHz power applications. The pattern microphotograph of single-cell MESFET is shown in Fig. 4. A cutaway view of the MESFET is shown in Fig. 5. The single cell consists of 28 interdigitated sources, 28 drains, and 52 gates with a total width of 2600 μm. The gate length is 1.5 μm. The n^+ source and gate are 1.0 μm apart and the n^+ drain and gate 2.0 μm apart. All source electrodes are connected to a large grounding electrode. An SiO_2 film is used for insulating the overlaid conductor from the source (see Fig. 5). The parasitic capacitance added by the crossover is designed to be less than 5 percent of the Schottky-gate capacitance.

B. Fabrication Process

An Fe-doped semi-insulating buffer layer and a sulfur-doped n-type layer are sequentially grown, in one step, on a Cr-doped semi-insulating substrate [11]. The device is fabricated on the n-type layer. The doping density and thickness of the n-type layer are 9×10^{16} cm^{-3} and 0.2 μm, respectively.

The detailed MESFET fabrication technique is the same as previously reported [6], except for an n^+ selective epitaxial process. The n-type layer outside the active area is etched down to the buffer layer. A 0.1-μm-thick SiO_2 film is deposited by a CVD of SiH_4 and O_2, and etched selectively to open windows for the interdigitated source and drain

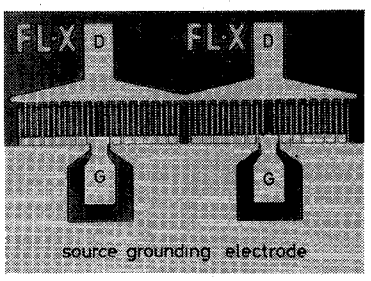

Fig. 4. Microphotograph of a single-cell MESFET.

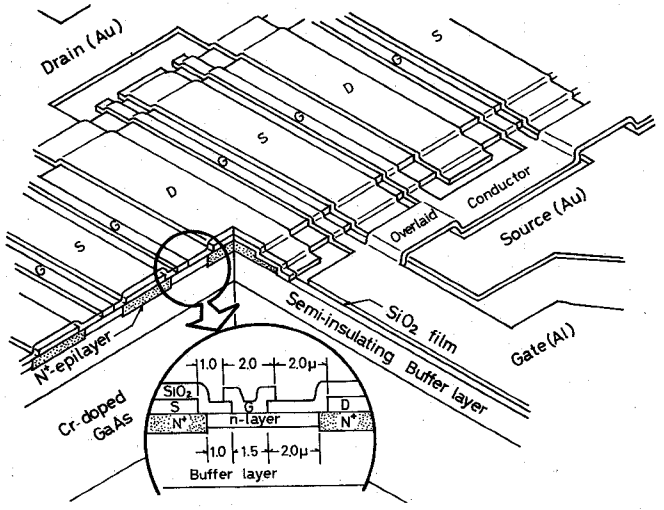

Fig. 5. Cutaway view of a MESFET.

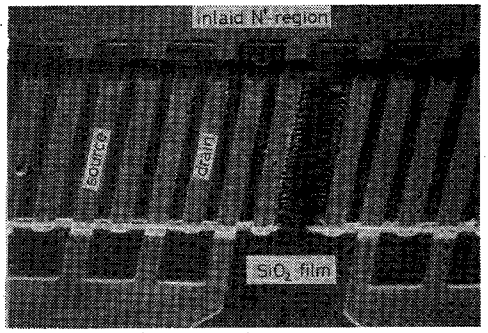

Fig. 6. Scanning electron microphotograph of the pattern after selective epitaxial growth of n^+ inlaid regions.

regions. The exposed GaAs layers are etched to a depth of 0.25 μm and these etched regions are just filled up again, as shown in Fig. 6, by sulfur-doped n^+ GaAs which is selectively grown by a $(C_2H_5)_2$ GaCl–AsH_3 system. The doping density of the n^+ region is about 3×10^{18} cm^{-3}.

This process is followed by an Au–Ge film deposition onto the wafer to make the source and drain electrodes. A contact resistivity less than 1×10^{-6} $\Omega \cdot$cm^2 has been easily obtained by introducing the inlaid n^+ region. After alloying these electrodes, a SiO_2 film is deposited and etched to open gate windows. Finally, an Al film is deposited and etched to make the overlaid conductor which connects a number of the Schottky barrier gates in parallel. A scanning electron micrograph of the MESFET center section is shown in Fig. 7.

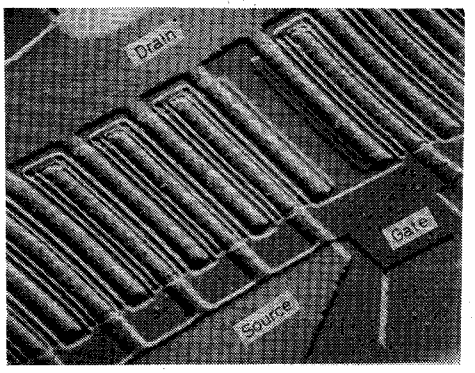

Fig. 7. Scanning electron microphotograph of a MESFET center section.

IV. Device Performance

Typical electrical characteristics of single and two-cell MESFET's are shown in Table I.

The test circuits for power measurements at 4, 6, and 8 GHz use microstrip lines on alumina substrates. The circuit at 6 GHz is shown in Fig. 8. The power measurement consists of several steps. Initially, the gate is fully reverse biased and a drain-source bias of 6 V is applied (no drain current). Next, the gate voltage is reduced until the drain current increases to about half the saturation value. Then the gate is driven by an input power of 10 dBm. Fine adjustments of input and output matching circuits are carried out by soldering open stubs at suitable locations on the microstrip lines until a reasonable power gain, expected from the small-signal s-parameter measurements, is obtained. Finally, the drain-source bias is increased to a desired value keeping the gate bias constant, and the input power is increased to an appropriate value. The large-signal input matching condition is very close to the image-matching condition for small-signal operation. However, since the output matching condition is different, a retuning of the output circuit is necessary for maximum output power.

The output power and power added efficiency $\eta_{add} = (P_{out} - P_{in})/P_{dc}$ are plotted each as a function of input power in Fig. 9 for a drain-source bias of 13 V. In a common source Class A operating condition, a two-cell MESFET delivered an output power as high as 2.7 W at 1-dB gain compression with 30.7-percent power added efficiency (η_{add}) at 6 GHz. Fig. 10 shows the output power and η_{add} at 1-dB gain compression as functions of drain-source bias voltage V_{ds} at 6 GHz. It is noteworthy that the output power at 1-dB gain compression ($P_{1\,dB}$) increases almost linearly with drain-source bias voltage up to 15 V. The burn-out drain-source bias voltage of a single-cell MESFET at 200-mA drain current is as high as 17 V; the relation between V_{ds} and the Schottky barrier gate breakdown voltage (V_{SB}) will be discussed in the Appendix. An arrow on the V_{ds} axis indicates the burn-out drain-source bias voltage of early MESFET's [6] without inlaid n^+ regions.

Third-order intermodulation measurements have been made to examine the linearity [12]. For a two-carrier test the output power at 1-dB gain compression was 27.8 dBm (0.6 W) for a single carrier at 6.2 GHz. The intercept

TABLE I
TYPICAL ELECTRICAL CHARACTERISTICS OF SINGLE AND TWO-CELL MESFET'S

Parameters and Test Conditions	Symbols	1 Cell	2 Cells
Gate Width	W_g	2600 μm	5200 μm
Drain Saturation Current at V_{DS}=5V, V_{GS}=0V	I_{DSS}	0.5 A	1 A
Transconductance at V_{DS}=5V, V_{GS}=-2V	g_m	160 m℧	320 m℧
Pinch-Off Voltage at V_{DS}=5V	V_P	4 V	4 V
Drain-Source Breakdown Voltage at V_{GS}=-2V	V_{dsB}	> 17 V	> 17 V

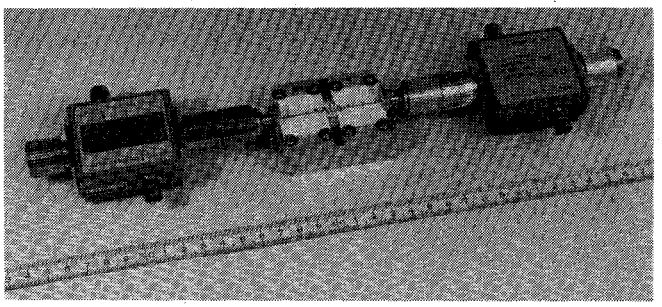

Fig. 8. Test circuit for power measurement at 6 GHz. The scale is calibrated in millimeters.

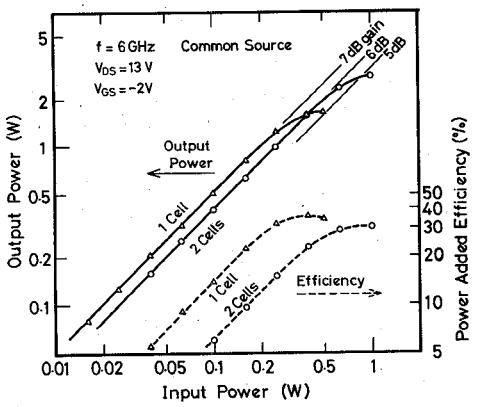

Fig. 9. Output power and power added efficiency versus input power at 6 GHz.

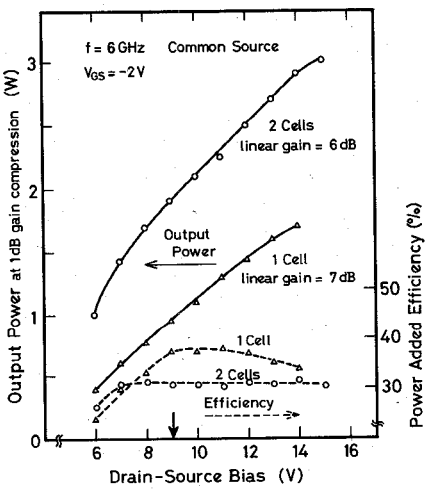

Fig. 10. Output power and power added efficiency at 1-dB gain compression versus drain-source bias voltage at 6 GHz.

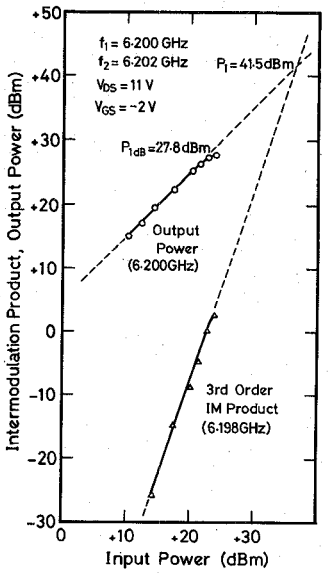

Fig. 11. Output power and third-order intermodulation products versus input power at 6.2 GHz.

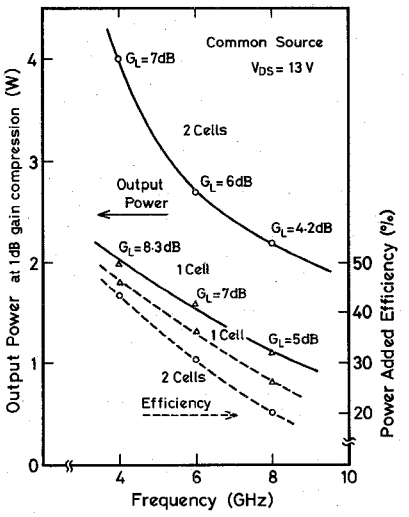

Fig. 12. Output power and power added efficiency at operating frequencies from 4 to 8 GHz.

point (P_I) for third-order intermodulation products was 41.5 dBm at 6.2 GHz, as shown in Fig. 11.

$P_{1\,dB}$ and η_{add} of single and two-cell MESFET's at operating frequencies from 4 to 8 GHz are shown in Fig. 12. At 4 GHz, $P_{1\,dB}$ = 4.0 W, G_L = 7 dB, and η_{add} = 43.5 percent are obtained from a two-cell MESFET. At 8 GHz, $P_{1\,dB}$ = 2.2 W, G_L = 4.2 dB, and η_{add} = 21.6 percent. In comparison, recent Si bipolar transistors delivered 1.5 W with η_{add} = 45 percent at 4 GHz, 1.5 W with η_{add} = 24 percent at 6 GHz [13], and 1.0 W with η_{add} = 25 percent at 8 GHz [14]. These results were achieved under common base Class *B* and *C* conditions which generally do not show good linearity. For linear amplification a Si bipolar transistor under Class *A* operation gave 0.5 W with η_{add} = 15 percent at 4 GHz [13].

Fig. 13 shows the temperature distribution of a MESFET chip (two-cell) observed by an infrared microscope at 4-W dc power dissipation and 25°C case temperature. The thermal

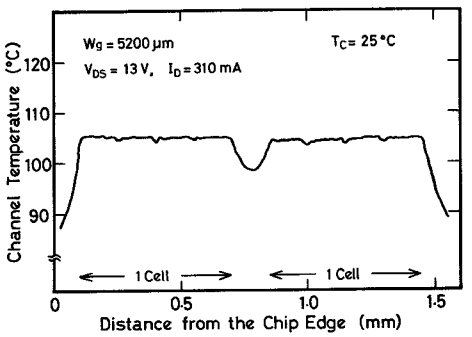

Fig. 13. Temperature distribution of a MESFET chip observed by an infrared microscope.

resistance was calculated to be about 20°C/W. Compared to Si bipolar power transistors, the MESFET shows a very uniform temperature distribution.

In order to examine the reliability of MESFET's, a life test of an amplifier with 1-W output power at 6.2 GHz has been carried out using a single-cell MESFET. After 1000 h no change has been found in the characteristics of the device.

V. Conclusions

High output power in *C* band and *X* band can be obtained from GaAs MESFET's by achieving a high drain-source breakdown voltage. The introduction of "inlaid" n^+ regions under source and drain electrodes contributes greatly to improve the drain-source breakdown voltage. The reported results are summarized as follows.

1) A power GaAs MESFET with a high drain-source breakdown voltage in excess of 17 V has been developed.

2) A selective GaAs epitaxial process was introduced to form the "inlaid" n^+ source and drain regions which can provide a high drain-source breakdown voltage and a low ohmic contact resistance.

3) It was found that the drain-source breakdown voltage is closely related to the source and drain configurations.

4) A 5200-μm-wide gate MESFET (two-cell) gave the following results.

$P_{1\,dB}$ = 2.2 W G_L = 4.2 dB η_{add} = 21.6% at 8 GHz

$P_{1\,dB}$ = 2.7 W G_L = 6 dB η_{add} = 30.7% at 6 GHz

$P_{1\,dB}$ = 4.0 W G_L = 7 dB η_{add} = 43.5% at 4 GHz

where $P_{1\,dB}$, G_L, and η_{add} indicate the output power at 1-dB gain compression, linear gain, and power added efficiency, respectively.

5) The intercept point for third-order intermodulation products was 41.5 dBm at 6.2 GHz (two-cell).

6) The temperature distribution of a MESFET chip (two-cell) was found to be very uniform at an operating condition of 4-W power dissipation and the thermal resistance was about 20°C/W.

Appendix

To avoid voltage breakdown, the following inequality has to be satisfied:

$$V_{ds} \leq V_{SB} - |V_{gs}| \qquad \text{(A1)}$$

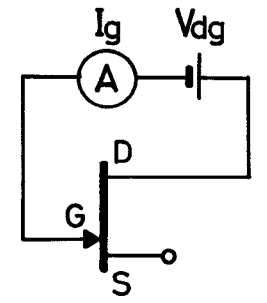

Fig. 14. Measurement of V_{SB} with the source electrode open circuited.

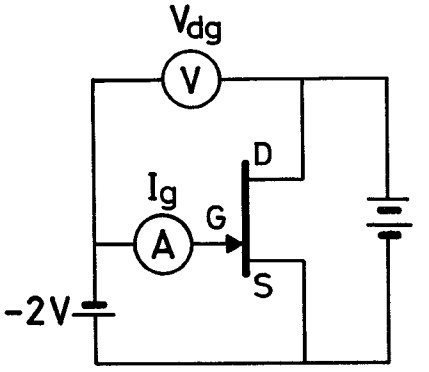

Fig. 15. Measurement of V_{SB} under the ordinary MESFET operating condition.

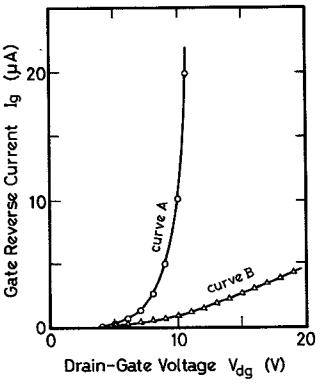

Fig. 16. Gate currents versus V_{dg} with the bias connections shown in Fig. 14 (curve *A*) and Fig. 15 (curve *B*).

where V_{ds}, V_{SB}, and V_{gs} represent the drain-source bias voltage, the Schottky barrier breakdown voltage, and the gate-source bias voltage. V_{SB} is usually measured with the source electrode open circuited as shown in Fig. 14. However, we believe that an appropriate method of measuring V_{SB} is as shown in Fig. 15. The reason is as follows. Curves *A* and *B* in Fig. 16 indicate the gate currents versus V_{dg} with the bias connections shown in Figs. 14 and 15, respectively. One may conclude $V_{SB} \simeq 10$ V from curve *A*. However, curve *B* indicates that V_{SB} approaches 19 V under the ordinary operating conditions. The maximum value of V_{ds} is 17 V from (A1) when $V_{SB} \simeq 19$ V. Our experiments agree with this value of V_{ds}. On the other hand, if the value obtained with Fig. 14 is used, the maximum value of V_{ds} becomes 8 V from (A1), which is too low compared with our experiments.

Conventional FET's without inlaid n^+ regions have a

drain-source breakdown voltage of approximately 7 V. When measured with the connection shown in Fig. 15, the gate current increased rapidly as V_{dg} approached 9 V because of the drain-source breakdown. As a result, the gate current versus V_{dg} became similar to the one obtained with Fig. 14. Thus there was no need to distinguish V_{SB} obtained by the two methods with conventional FET's.

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Some Aspects of GaAs MESFET Reliability

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Abstract—**The results of a short study into the reliability and failure modes of GaAs MESFET's are presented. Two failure modes have been observed during this study and improved fabrication techniques that reduce their occurrence have been examined. The results obtained indicate that extremely reliable devices can be manufactured with a predicted mean time to failure in excess of 10^7 h at junction temperatures of 70°C. Room-temperature life tests in excess of $\frac{1}{2}$ million device hours lend support to these predictions.**

I. INTRODUCTION

THE past few years have seen the emergence of the GaAs MESFET as a microwave transistor of tremendous potential. It combines low noise, high gain, and large dynamic range at frequencies unlikely to be reached by bipolar devices. There have been many papers published on its applications [1]–[3] and its variants [4]–[8], but little has been reported on the long-term reliability of the device. With the imminent prospect of MESFET amplifiers being used in space applications [9], device reliability is of prime importance.

This paper presents the results of stress testing on a number of *X*-band devices with different metallization systems. Four different ohmic contact systems were tested:

1) gold/germanium (Au/Ge);
2) indium/gold/germanium (In/Au/Ge);
3) nickel/gold/germanium (Ni/Au/Ge);
4) platinum/gold/germanium (Pt/Au/Ge).

The devices with Au/Ge metallization had a passivation layer of silicon monoxide covering the channel area and parts of the drain and source contact, and the Pt/Au/Ge devices had an overplate of a thin chromium (Cr) layer and a thicker Au layer.

The tests performed included reverse biasing of the gate diode at an elevated ambient temperature, thermal cycling from −65 to +150°C, ac modulation of the drain current by application of gate volts to turn the device on and off,

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